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Design, Analysis & Simulation of 30 nm Cylindrical Gate all around MOSFET

Tarun Kumar Sachdeva[1],Dr. S.K. Aggarwal[2] , Dr. Alok K Kushwaha[3]

Research Scholar, EEE Department, YMCAUST, Faridabad[1]

Professor, EEE Department, YMCAUST, Faridabad[2]

Professor& Asst. Dean Academic, Waljat College of Applied Science, Muscat, Oman[3]

Abstract: Cylindrical gate all around (GAA) MOSFET is a drastic invention and a potential candidate to replace conventional MOSFET, as it introduces new direction for transistor scaling without hindering the device performance.In this work, electrical characteristics of cylindrical GAA (CGAA) MOSFET at 50nm channel length (Lg), 10nm channel thickness (t_{si}) are systematically analysed. Various electrical characteristics such as On current (I_{ON}), subthreshold leakage current (I_{OFF}), the threshold voltage (V_{th}), DIBL are calculated and analysed at various device design parameters.All the device performances of Cylindrical GAA MOSFETs are investigated through Atlas device simulator from Silva co.

Keywords: Cylindrical gate all around (GAA) MOSFET, subthreshold leakage current (I_{OFF}),

1. INTRODUCTION

The aggressivescaling of CMOS technology has been the attention of electronic industry in the last few decades. The main propel for scaling is the necessity of achieving higher packing density, intensifyingthe performance of SOI chips, and cost effective electronic devices. However, the scaling of the CMOS transistor comes on the cost of raising several flawed such as drain-induced barrier lowering, hot carrier effects etc.

These flawsalso known as short channel effects, have a large impact on the performance on the circuits, and therefore they limit the expected performance enhancement [1]-[2].To overcome these flaws, new circuits and design techniques are mandatory to utilize the edge of the newer technologies.

Some multi-gate silicon on insulator (SOI) technology has also been proposed for promising solution to replace the conventional MOSFET [3]. However, the cylindrical gate all around (CGAA) MOSFET is one of the new technologieswhich further enables the scaling without hampering the device performance [4][5].Since due to higher drive current and shorter length, Cylindrical GAA MOSFETs can achieve higher packing density as compared to the other multiple-gate MOSFETs.

Also, cylindrical gate-all-around (CGAA) MOSFETs in which the gate oxide and the gate electrodes wrap around the channel region exhibit excellent electrostatic control of the channel, no floating body effect,stoutness against SCEs, better scaling options, ideal sub threshold swing as compared to other multi-gate MOSFETs [6]. Hence, the CGAA MOSFETs are a brilliant solution for nanoscale technology CMOS devices [7].

Also various important device parameters like threshold voltage (V_{th}), and on-off ratio (I_{ON}/I_{OFF}), are very much sensitive to the device geometry such as channel length (Lg), channel thickness (t_{si}).In this paper, various electrical parameters, like threshold voltage (V_{th}), drain current (I_D) are analytically presented.

2. DEVICE STRUCTURE AND SPECIFICATION

The schematic diagram of the Cylindrical GAA (CGAA) MOSFET structures used for simulation is shown in Fig. 1.This structure is implemented using Atlas Silvaco tool. The radial directions are assumed to be along radius and lateral direction along z-axis of the cylinder as shown in Fig. 1.

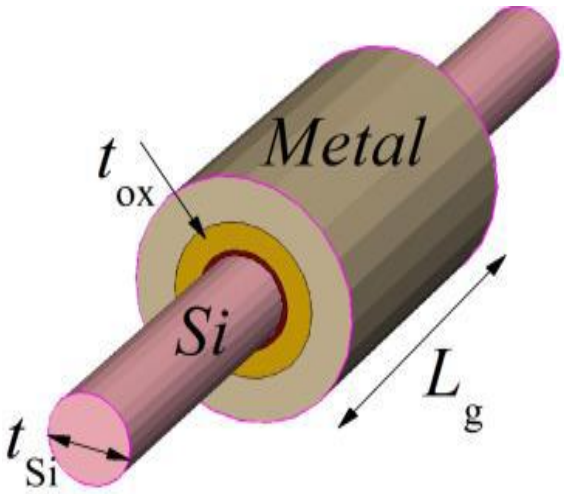

Fig 1: Schematic Structure of Cylindrical Gate All Around (GAA) MOSFET

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The details of device physical parameters used in the structure are shown in Table 1.SOI substrate in GAA MOSFETs having n-type channels. The Length of the gate (Lg) is 30nm with work function 4.4 eV. We have taken diameter (t_{si}) of 10nm. We use SiO_2 in gate oxide with thickness (t_{ox}) 1 nm.

Table 1: Device Dimensions &Dopings

Parameter	Value
Gate Length (Lg)	30nm
Radius (t_{si}/2)	5nm
OxideThickness (t_{ox})	1nm
Channel Doping	$1.0x10^{18}$ cm^{-3}
Source Doping (N_D)	$1.0x10^{20}$ cm^{-3}
Drain Doping (N_D)	$1.0x10^{20}$ cm^{-3}

The source/drain extension doping profile was set as Gaussian with the peak concentration of $1.0x10^{20}$ cm^{-3}.
Fig 2 shows the cross sectional view of cylindricalGAA MOSFET of channel length 30 nm has been used in simulation.

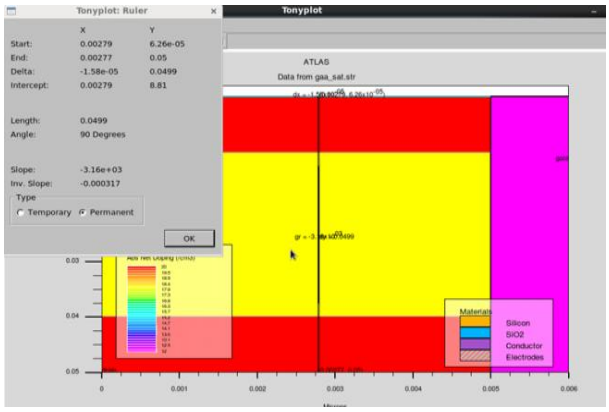

Fig 2: Cross sectional view of GAA structure for channel length (Lg)

Fig 3 shows the cross sectional view of GAA structure for silicon thickness of radius(t_{si}/2) 5nm and oxide thickness of 1nm has been used in simulation.

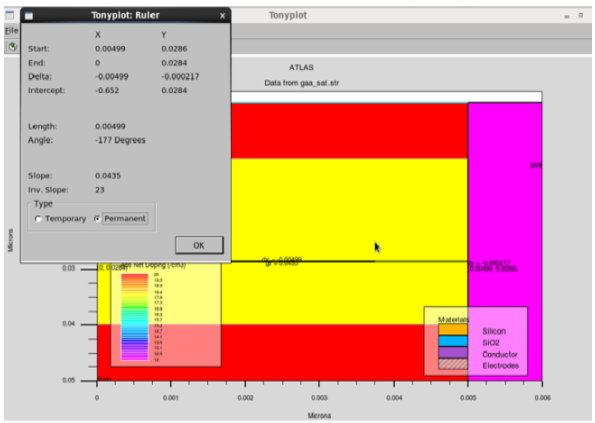

Fig 3: Cross sectional view of GAA structure for Oxide thickness (t_{ox})& Silicon thickness (t_{si})

Fig 4 shows the Uniform donor(N_D)doping profileplot between source and drain of fixed charges $1x10^{20}$ cm-3 is used in the simulation to avoid abrupt junction.The metal gate work function $\varphi_{M=}$ 4.4 eV has been considered.

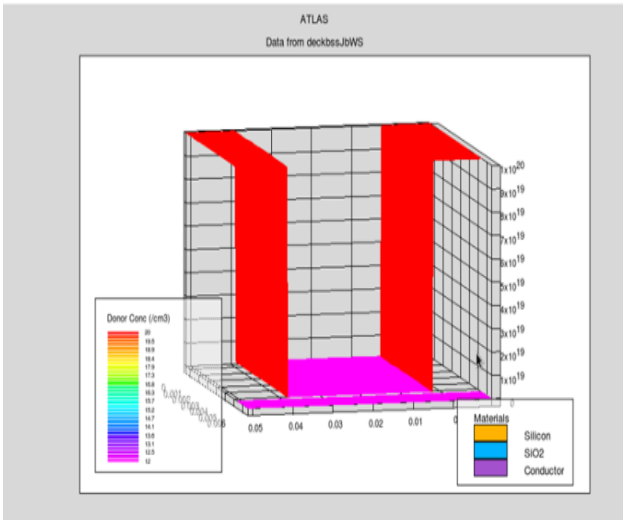

Fig 4: Donor Concentration Graph

3. RESULTS AND DISCUSSION

Fig 5 demonstrates the transfer characteristics of GAA MOSFETs. Simulation was done with various drain voltages.

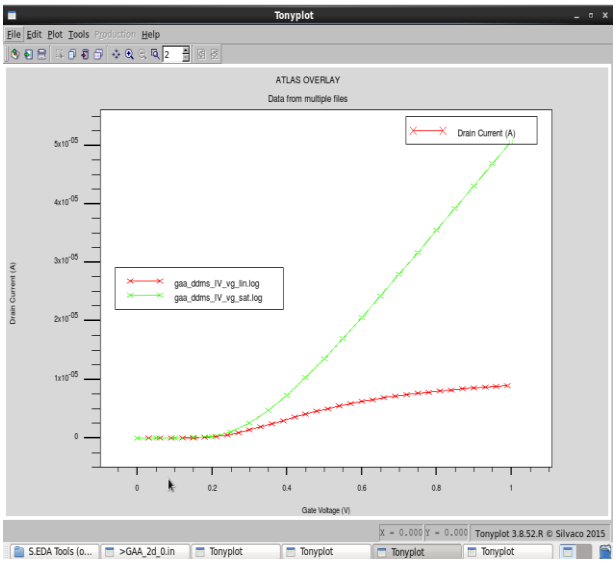

Fig 5: Drain current (I_D) versus Gate Voltage (V_{GS}) plot for V_{DS} =1 V and 0.1 V

GAA MOSFET threshold voltage (Vth) extraction was performed based on a constant current definition which is universally adapted to measure. During simulation we consider a constant current level of$1x10^{-7}$ A/ m.Fig 6 shows the transfer characteristics of GAA MOSFET for various Gate voltages. DIBL was defined as the difference in threshold voltage when the drain voltage was increased from 0.1 to 1 V.

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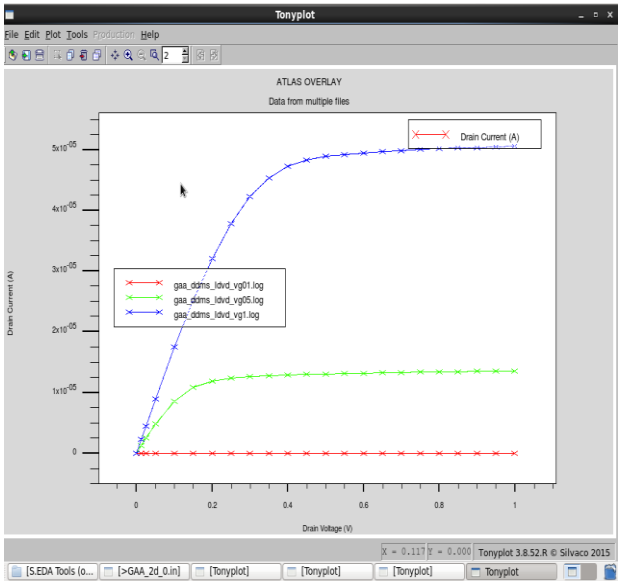

Fig 6: Drain Current (I_D) in log scale as a function of Gate Voltage (V_{GS}) for V_{DS} =1 V and 0.1 V

Driving current $I_{ON}$and I_{OFF} were analysed for various Gate Voltage (V_{GS}). Fig 7 shows the driving current I_{ON} was obtained at V_G=1.0 V and I_{OFF} was obtained at V_G= 0.1 V.

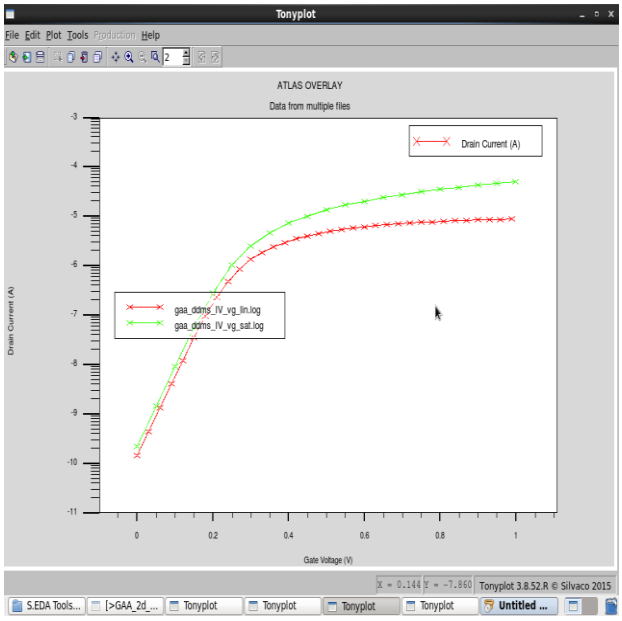

Fig 7: I_{ON}& I_{OFF}current for different Gate voltage V_{GS}

The Result of Simulation were summarised in Table II.

Table II: Simulated value of Electrical Characteristics of the structure

Parameter	Value
V_{TH}	0.17 V
SS	0.06159 mV/dec
DIBL	0. 0182544 mV/V
I_{ON}	7.74e-5 A
I_{OFF}	1.74e-10 A

4. CONCLUSION

To reduce the short channel effects (SCEs) and improving the device reliability, GAA MOSFET is proposed. GAA MOSFETs showsrefinement in almost every aspect such as subthreshold swing (SS), OFF state current (IOFF) and DIBL. Better suppression of SCEs and an improvement in the device reliability has been observed through the simulation results.

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